Nonlinear III-V HBT Compact Models: Do We Have What We Need?

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Abstract— **Within the large body of literature on models for III-V HBTs it now seems possible to find compact formulations with extractable parameters that model all important device characteristics. Predictions are as accurate as possible given the limitation of quasi-static host simulators. Some recommended strategies for extraction of parameters for certain formulations are given. Despite accurate formulation, some aspects may be better left out of models in the interest of expediency, with no significant reduction of final performance. Transit time remains difficult, and limitations of simulators swamp discrepancies between measurement and predictions of even apparently-precise models. It is concluded that compact models, if not simulators, are as physically precise as we should bother to make them.**

I. Introduction

MODELING Heterojunction Bipolar Transistors, particularly in the III-V family, is a challenge that has spawned over 100 publications in well-respected journals over the last 10–15 years. The majority address the design of a compact model, typically physically-based, for use in contemporary simulators such as SPICE or ADS, and the extraction of parameters for such models. One might expect that by now the literature would contain enough wisdom for a satisfactory model to have become clear, even if all facets of this Gestalt-model were not to have been collected in one citation. This proposition is examined here.

II. Dc Model

Most complete, large-signal, compact, III-V HBT models in the literature (for example see [1]–[7]) employ a small, separate subcircuit to model self-heating (at least in the case of a single device in thermal isolation from other dissipators), after the fashion of the VBIC model[8]. The dc collector current in forward-active operation is computed from three voltages, the (intrinsic) base-emitter voltage v_{be_i}, the (intrinsic) base-collector voltage v_{bc_i}, and the voltage found from the thermal subcircuit and which represents instantaneous device temperature, v_{Tj}.

Figure 1 is a Gummel plot for an HBT with an emitter area of $16\mu m^2$ for substrate temperatures of 15–105C. Note that both the "extrinsic" and "intrinsic" data are plotted. It is immediately obvious that the curvature of the extrinsic data must be significantly altered by the parasitic resistances and device self-heating. These go in opposite direction, and the curvature of the measured result is deceptively mild.

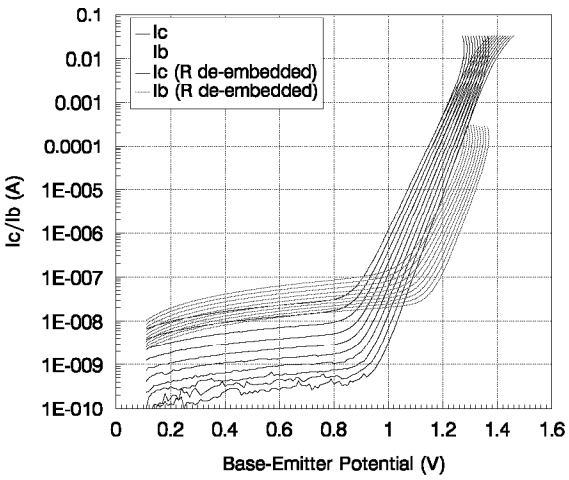

Fig. 1. Gummel plot for an InGaP/GaAs HBT with an emitter area of $16\mu m^2$ for substrate temperatures of 15–105C.

The UCSD model[5] has the transfer-current form

$$I_{cc} = \frac{I_{sf}(T_j)e^{\frac{V_{be_i}}{N_f V_T}} - I_{sr}(T_j)e^{\frac{V_{bc_i}}{N_r V_T}}}{q_1 \frac{(1+\sqrt{4q_2+1})}{2} + I_{sa}(T_j)e^{\frac{V_{be_i}}{N_a V_T}} + I_{sb}(T_j)e^{\frac{V_{bc_i}}{N_b V_T}}} \quad (1)$$

where base-width modulation or Early effect and high-level injection/knee-current or Webster effect are modeled as in the case of silicon, should they be significant, through the action of q_1 and $\frac{1}{2}(1+\sqrt{4q_2+1})$ respectively; the saturation currents may be adjusted dynamically for junction temperature T_j according to [2]:

$$I_s(T_j) = e^{[\ln(I_s)+(1-\frac{T_{ref}}{T_j})\frac{T_s}{T_{ref}}]} \quad (2)$$

Numerical fitting applied initially to data at each temperature, and subsequently to all the Gummel plots simultaneously, yields saturation current variation as shown in figure 2, and finally the agreement shown in figure 3. In this fit, the Webster term is switched off ($q_2 = 0$) and the reverse terms negligible, but the forward "heterojunction" term in the denominator is required for the equation to fit for

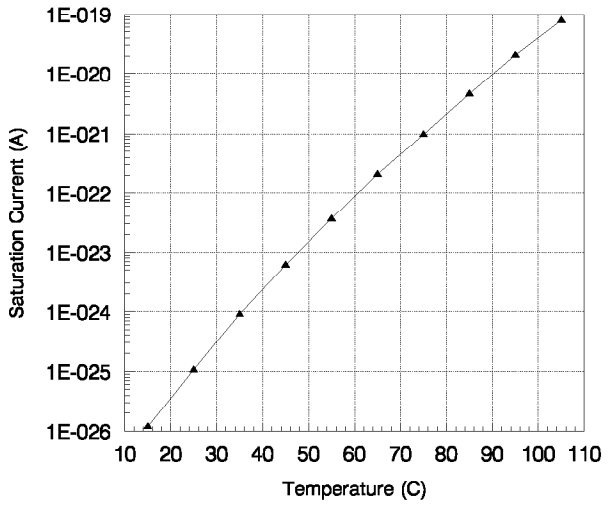

Fig. 2. Plot of saturation current I_{sf} against temperature, resulting from numerical fitting of equations 1 and 2 to the measured data in figure 1.

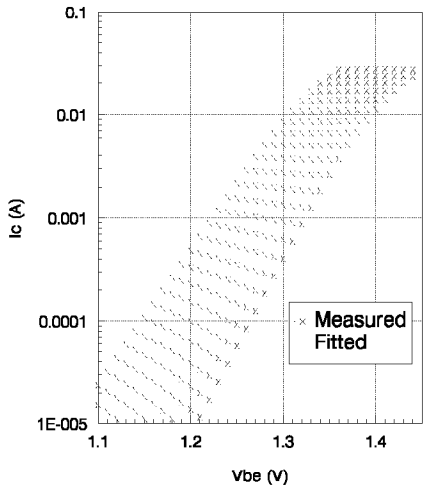

Fig. 3. Plot of measured data and model prediction of collector current from equations 1 and 2.

higher current densities. Almost as good a fit can be obtained, for practical current densities, without the forward "heterojunction" term but with the Webster term pressed into service in its place.[1] In summary, dc, collector-current models are excellent, but absolutely demand precise allowance for temperature and terminal resistances. For the above fit, R_{th} and R_{ee} are required and must be accurate to a few percent; R_{bb} is less critical as its effect is smaller, and R_{cc} becomes significant only in saturation characteristics.

The extraction of thermal resistance, R_{th}, has been recently addressed elsewhere.[9] Experience suggests that the extraction of R_{ee} is most effective using a technique based on [10] but additionally taking care to repeat extrapolation in the reciprocal-current domain for separate frequency-temperature pairs and *with allowance for device self-heating*. The reader must take the author's word for this in the interest of respecting the page limit.

The modeling of base current is less prominent in the literature, and even multi-diode models such as that in [1] achieve slightly less exact a fit than in the case of collector current. This may stem from the fact that many HBT processes suffer relatively large shifts in base-current characteristics with time. The reader must also take the author's word for this in the interest of respecting the page limit.

A recent discussion of breakdown appears elsewhere,[14] and so is omitted here.

III. Charge-Storage Model

Suitable calculations made on measured S-parameter data readily distinguish device capacitance and transit time.[11], [12] With less reliability, base and collector transit times may be distinguished.[13] Simulators running compact models ultimately need to know node currents (and conductance and transconductances), as well as node stored charge (and capacitance and transcapacitances) as a function of node voltages. It is critical to note here that once equations are selected to model the stored charge arising from capacitive and transit effects, their return values must be assigned to nodes (branches) and all the charges on any given node (branch) summed and treated identically. Thus *it will never be possible to distinguish the provenance of a charge from S-parameter data derived from the model* as was the case with measured data. E.g., figure 6 can never be reproduced faithfully using data from simulation.

In selecting equations to model charge stored in capacitance and transit, approaches in the literature are less unified. The UCSD model, whose charge storage part is largely attributed to Camnitz[4], uses a reasonably well-accepted model for capacitance but with the addition of the possibility that C_{bc} will be modulated by collector current. Figure 4 shows the variation of C_{bc} with both voltage and current. The latter effect is perceptible, but barely so. The variation with voltage is well modeled by the usual SPICE equation with linear extension for voltages approaching the built-in potential, and with a minimum value reached at punch-through. Various publications implement this differently (for example [1] uses a root-of-sum-of-powers smooth maximum function, [5] a continuous but not differentiable piecewise function) but the effect is equivalent. Figure 5 illustrates the UCSD-style piecewise model.

[1]This is physically "incorrect", as the Webster term effectively forces the current in the absence of resistive and thermal effects towards an asymptote with slope corresponding to an ideality factor of 2, but the UCSD-model "heterojunction" term does not constrain the asymptote slope.

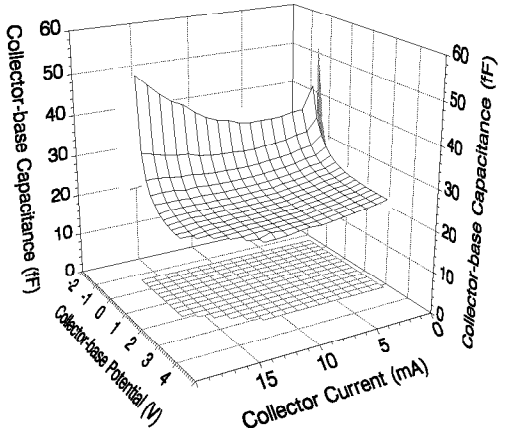

Fig. 4. Plot of C_{bc} as a function of voltage and current. Note the projections on the axis planes that assist visualization of the surface.

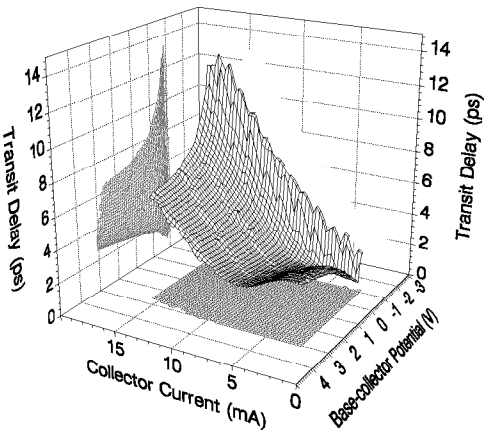

Fig. 6. Plot of measured transit time ($\tau_B + \tau_C$) as a function of voltage and current, again on a 16μm^2 HBT. Note the projections on the axis planes that assist visualization. Values have been computed from S-parameter data measured under short pulsed-I/V conditions.

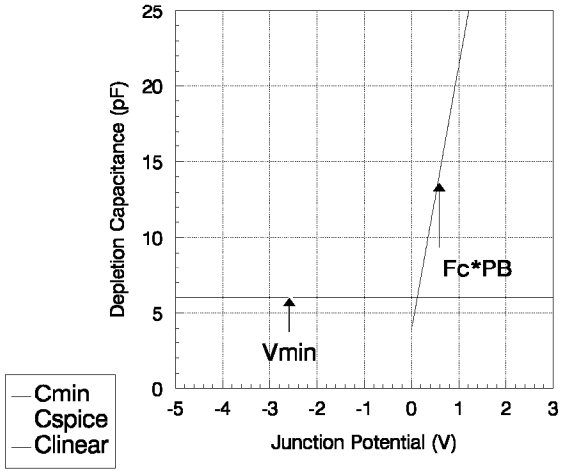

Fig. 5. Plot of depletion capacitance against junction voltage, showing the "discrete regions" (minimum or punched-through, SPICE-like, and linearly extrapolated) involved. The final capacitance follows the SPICE formulation in the middle region.

Figure 6 is a surface plot of transit time extracted in the usual way[15] from an HBT similar to that used previously. No completely suitable modeling formulation seems to be available in the literature. The best formulation is perhaps the strongly physical one in [16], but being chiefly aimed at silicon devices, it does not incorporate "f_T peaking", which accounts for the dip visible in figure 6 for mid-currents and higher voltage. The UCSD model in [5] does potentially incorporate f_T peaking but otherwise relies on equations that have no strong physical basis, and whose parameters are difficult to extract. Apart from the peaking phenomenon, however, equations culled from [16] are effective at reproducing the data and have extractable parameters.

Difficulties can arise because transit charge storage is a function of temperature. Realize that the small-signal data from which points on the surface in figure 6 are computed has been measured across a range of bias values. If carried out with steady-state rather than pulsed bias, the device temperature would vary significantly across the same surface. Thus pulsed-S-parameters should used to obtain isothermal data.

A new transit-charge formulation[2] that very faithfully reproduces the data in figure 6 yields only a fair model. Because charges are superimposed, the model can never act as did the device even if it "knows" both capacitive and transit charges exactly. As example we might compare transit frequency (refer to figures 7 and 8): The agreement is fair to poor, not excellent like the values that went into the model. A more rigorous comparison involves looking at devices of different structure, parameters other than transit frequency[3], and circuits as well as discrete transistors, and cannot appear here.

IV. Conclusions

HBT models can be "excessively" accurate, including effects that may not be perceptible in devices. Model simplification in the interest of computational efficiency is appropriate in this case.

There is published evidence of phenomena operating in III-V HBTs that have not been addressed in the modeling literature, and so models do not prop-

[2]The new formulation is not yet in the public domain.

[3]The use of transit frequency represents the selection of a weighting scheme for scalar comparison of the 4 complex numbers that comprise 2-port S-parameters at each bias.

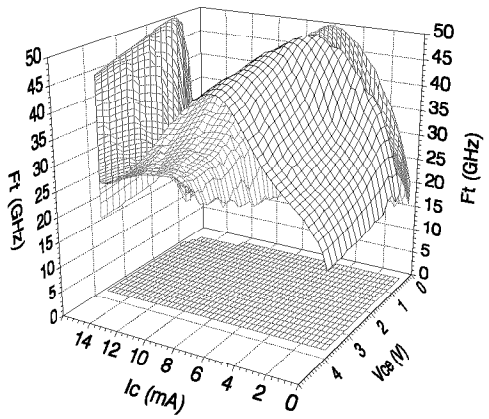

Fig. 7. Surface plot of transit frequency extracted from the same data used for figure 6.

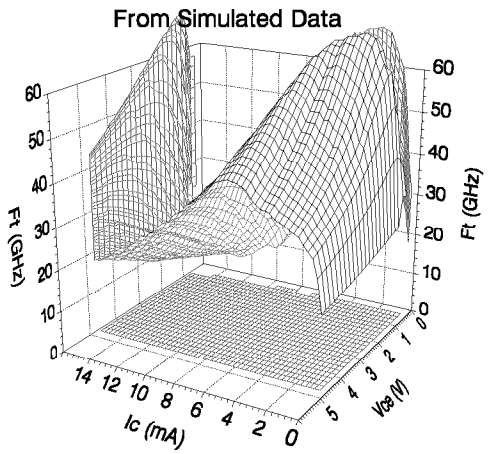

Fig. 8. Surface plot of transit frequency extracted from S-parameters obtained from a compact model fitted to the data used for figure 6, in which both capacitances and transit times are accurately modeled.

erly embody device response in such areas as base current for higher junction current density, or fine structure of collector current as a function of base-collector voltage. It could be argued that these effects barely impact many designs, or that designers do not expect such precision from simulations.

It has been shown that simulator inability to properly model transit charge can dominate prediction error. *This can negate any benefits expected from a superior model formulation.*

It is suggested that a good, if not perfectly satisfactory, model can be composed from what is available today in the literature. This conclusion might not hold true for a model that is not constrained to be quasi-static.

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